POWER COMBINING IN AN ARRAY OF MICROWAVE POWER RECTIFIERS*

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Abstract

To obtain useful power levels for proposed free-space microwave power transmission applications, numerous rectifier outputs are interconnected in series and/or parallel to share a common DC load. This work analyzes the resultant efficiency degradation when identical rectifiers operate at different RF power levels as caused by the power beam taper. The efficiency degradation is nearly identical with series and parallel combining and a closed form analytical model provides results which are similar to a detailed computer simulation model.

Introduction

In proposed applications of free-space microwave power transmission, large amounts of microwave power must be efficiently converted to DC. Numerous GaAs Schottky rectifier circuits, fed from individual receiving elements in a planar array pattern called a "rectenna", share a common DC load to achieve useful power levels. The rectifier outputs can be combined in series and/or parallel to enhance the voltage and/or current levels respectively.(1-2)

A fundamental question in this receiving, rectification and power combining process is caused by the power taper of the incident microwave beam. Since the output (DC terminal) characteristics of the rectifier are power dependent, rectifiers at different power levels that share a common DC load cannot be operated at optimum conditions. In this work the efficiency degradation that results when an array of microwave power rectifiers shares a common DC load is evaluated for the first time.

Methodology

In this section we present the method used for determining the loss in power which results when several rectenna elements, operating at different RF power levels, are connected in either series or parallel, following a method developed by Appelbaum et. al.(3) for photovoltaics. We show in Fig. 1 a general V-I output characteristic of two rectenna elements, along with constant power contours. The V-I characteristic can be determined by either a circuit analysis of the rectenna element, by a computer simulation or by direct measurement of the output voltage and current for several load resistances. It is assumed that the V-I characteristics are a function of some parameter θ (in our case incident RF power), that is

$$V = f(I,\theta) \quad \text{or} \quad I = h(V,\theta) \tag{1}$$

so that the power output is

$$P = IV = I\, f(I,\theta) = V\, h(V,\theta). \tag{2}$$

Given the V-I characteristics, it is possible to determine the operating point for maximum power output for both elements, i.e. V_{m1}, I_{m1} and V_{m2}, I_{m2}. The difference in the maximum power of N isolated rectenna elements and the maximum power when they are DC interconnected is defined as the power combining loss:

$$(\Delta P)_c = \sum_{j=1}^{N} (P_j)_{max} - (P_{max})_c \tag{3}$$

and the ratio:

$$\Delta P_c / \sum_{j=1}^{N} (P_j)_{max} \tag{4}$$

as the power combining inefficiency. When several rectenna elements are interconnected in series, the maximum array power can be expressed as

$$(P_{max})_s = I_m \sum_{j=1}^{N} f(I_m,\theta_j) \tag{5}$$

and for a parallel interconnection

$$(P_{max})_p = V_m \sum_{j=1}^{N} h(V_m,\theta_j) \tag{6}$$

These equations are very general and it is desirable to apply them to two cases of special interest with rectenna arrays.

First consider an array of elements whose output terminal behavior can be represented by an internal voltage source V_j in series with a resistance R_j, or the load line is linear with both V_j and R_j a function of the RF incident power. In the case of an array of series connected cells, the power combining inefficiency is given by:

$$\frac{(\Delta P)_s}{P_{max}} = \frac{\sum_{j=1}^{N} V_j^2/R_j - \left[\sum_{j=1}^{N} V_j\right]^2 \Big/ \sum_{j=1}^{N} R_j}{\sum_{j=1}^{N} V_j^2/R_j} \tag{7}$$

and in the case of parallel connected cells:

$$\frac{(\Delta P)_p}{P_{max}} = \frac{\sum_{j=1}^{N} V_j^2/R_j - (\sum_{j=1}^{N} 1/R_j)(\sum_{j=1}^{N} V_j/R_j \div \sum_{j=1}^{N} 1/R_j)^2}{\sum_{j=1}^{N} V_j^2/R_j} \tag{8}$$

A second more restrictive case occurs if all the internal resistances are the same for the rectifiers of the array. It can be shown that the power combining inefficiency becomes the same for parallel as well as for series connection and is given by:

$$\frac{\Delta P}{P_{max}} = 1 - \frac{(\sum_{j=1}^{N} V_j)^2/N}{\sum_{j=1}^{N} V_j^2} = 1 - \frac{(V_{av})^2}{(V^2)_{av}} \tag{9}$$

This is an interesting and useful result, namely that the power combining inefficiency of an array of elements operating at different power levels is nearly indepedent of the way in which they are interconnected (series or parallel).

Microwave Power Rectifier Circuit Models

In order to evaluate the power combining inefficiency with the equations developed previously, an accurate output equivalent circuit model of the conversion circuitry is needed. This was obtained using two independent approaches. First an approximate closed form circuit model of the rectifier was developed assuming an ideal diode and lossless circuit elements. The output equivalent circuit was then obtained analytically. Second a more precise computer simulation model was used, and the output equivalent circuit was obtained by varying

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the DC load resistance and plotting the resultant output load line.

While numerous rectifier circuits are possible, a single shunt model diode rectifier circuit has proven most useful in the development work to date,[2] and has been assumed in our work. An idealized equivalent circuit of this rectifier is shown in Fig. 2A, where the filter at the input should prevent any of the DC current and harmonics to flow back through the antenna resistance R_s, but allow current flow at the fundamental RF frequency ω. The function of the filter at the output is not only to prevent AC components to appear across the load terminals but also to allow harmonic currents to flow. The output filter should allow the even harmonics to flow without any voltage drop, should prevent current flow at any of the odd harmonics and should allow DC current flow. The above characteristics of the input and output filters can be obtained with the impedance shown in Figs. 2B and 2C respectively.

Two possible implementations of realizing filters with the above characteristics as shown in Fig. 3. In Fig. 3A the elements L_3, C_3, L_5, C_5, . . . , form parallel resonant circuits which are open circuited at the odd harmonics 3ω, 5ω, . . . respectively. The capacitor C_1 is used for preventing DC current flow as well as for series resonating L_3, C_3, L_5, C_5, . . . at the fundamental frequency ω. The L_2, C_2, L_4, C_4, . . . elements in the output circuit are series resonant at the even harmonics 2ω, 4ω, . . . respectively. The inductance L_0 is assumed to large enough such that the current I_L is mainly DC current. Thus I_1 is comprised entirely of fundamental frequency, while I_2 would consist of a DC current plus even harmonics. In Fig. 3B the output filter is replaced by a non-dispersive, $\lambda_0/4$ long transmission line terminated with a large capacitor.

The circuit analysis of these rectifiers circuits is identical and results in the output load line characteristics given in Fig. 4. From the DC load terminals the ideal rectenna element behaves as a DC voltage source of amplitude $\pi/4\ V_s$ and internal resistance of $\pi^2/8\ R_s$ where V_s is the peak amplitude of the RF source driving the rectifier and R_s is the source internal RF resistance. With this model the optimum DC load resistance is $\pi^2/8\ R_s$ and under this load 100% conversion efficiency is obtained.

This ideal efficiency has been achieved because it was assumed no losses in any of the circuit components or in the diode. Since these losses can be minimized by choosing a rectifier diode with small forward drop and small series resistance and high Q circuit elements, it is expected that the closed form conversion circuit model would be a good approximation for a high efficiency rectenna element. Additional factors to be considered are the diode non-linear depletion layer capacitance and package parasitics.

A computer simulation model is needed to handle these important factors and is shown in Fig. 5. It was decided to select reasonable diode parameters and to keep a 75 ohm RF impedance level throughout the circuit. A five stage lumped low pass Chebyshev filter was designed for the input and two stage smoothing filter at the output. In order to obtain conversion efficiencies above 80% input and output transmission lines were added between the mounted diode and filters, with the input line of particular importance. With this model, the incident power is varied by changing the value of the amplitude of the voltage source. The efficiency decreases from 84% at 2W incident power, to 75% at 0.2W, principally due to the diode turn-on voltage.

Output load line characteristics were obtained at various power levels by varying the load resistance, and plotting the resultant output DC load line characteristics. The load line for the computer simulation model of Fig. 5 obtained by only varying the output load resistance from 5 to 1500 ohms (instead of fixed at 75 ohms) is shown in Figure 6 for various power levels. Note that the computer model also results in a highly linear load line with similar characteristics to the closed form model.

Power Combining Inefficiency Results

A number of cases were calculated to arrive at a comparison between parallel and series power combining inefficiency with the computer simulation model and to evaluate the usefullness of the closed form analytical model. In performing these calculations discrete probability densities were used with sixteen categories of input power ranging from .5 to 2.0 watts in .1W steps. The power range was chosen to be comparable to the majority of rectenna elements in proposed solar power satellite (SPS) applications. With the computer simulation model, the output equivalent circuit parameters were obtained at each power level using the power dependent output load line.

Five cases presented for illustrative purposes are shown in Table 1. The first three cases are useful in evaluating diffraction effects with a serrated rectenna,[4] while the latter two are appropriate for evaluating power beam taper effects. A firm conclusion is that parallel and series power combining inefficiencies are nearly identical, and that the closed form model underestimates the power loss due to operation into a common load only slightly (by ~ 10% of the power combining inefficiency). The latter two cases shown indicate that the power combining inefficiency at the edge of a rectenna due to the incident power beam taper can be quite significant.

Summary

The power combining inefficiency is quite insensitive to the details of the conversion circuitry with highly efficient rectifiers, as indicated by the close numerical agreement using the closed form analytical model and the detailed computer simulation model. Unlike with photovoltaics, there is little difference between series and parallel DC combining, as the output load line characteristic of the microwave power rectifier is quite linear. The methodology can be extended to other parameter variations besides power level in evaluating the efficiency degradation dependence upon diode and circuit parameter tolerances.

References

1. W. C. Brown, "The Technology and Application of Free-Space Power Transmission by Microwave Beam", Proc. IEEE, Vol. 62, pp. 11-25, Jan. 1974.
2. W. C. Brown, "Electronic and Mechanical Improvement in the Receiving Terminal of a Free-Space Microwave Power Transmission System", NASA-CR-135194, Aug. 1977.
3. J. Appelbaum, J. Bany and A. Braunstein, "Array Power Output of Non-Identical Electrical Cells", 12th Annual Intersociety Energy Conversion Engineering Conference (IECEC), pp. 1686-1692, 1977.
4. Raytheon Company, "Rectenna Technology Study", Report PT-5155, March 1978.

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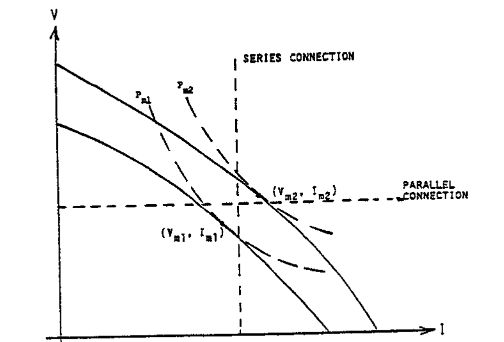


Fig. 1 Series and Parallel Interconnection of Two Different Rectifiers Illustrating Power Combining Inefficiency

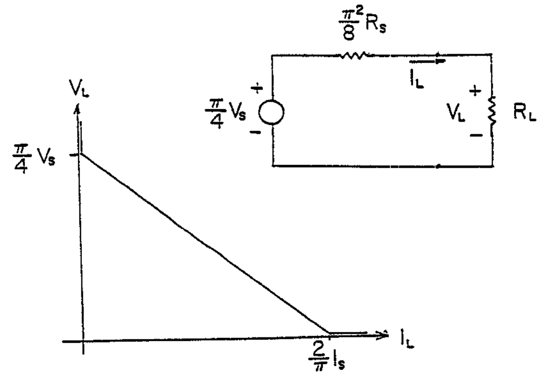


Fig. 4 DC Equivalent Circuit and Load Line Characteristic for Closed Form Model of Rectenna RF to DC Conversion Circuitry

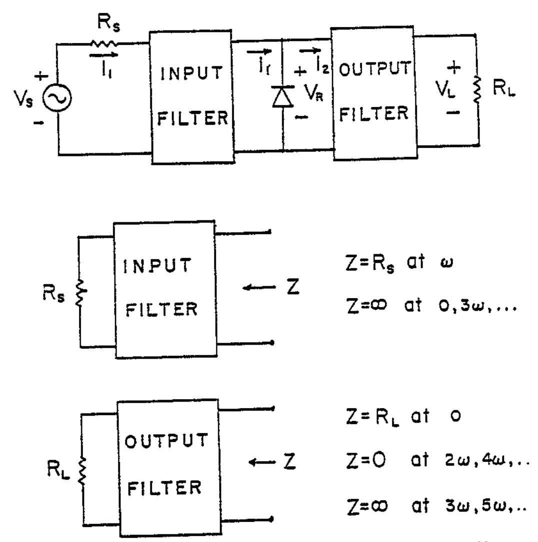
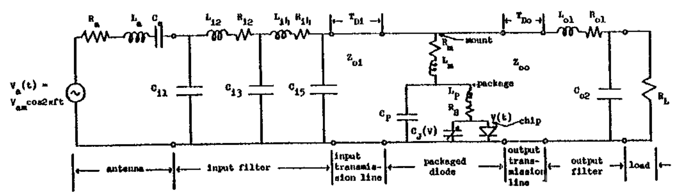


Fig. 2 Rectifier Circuit with Input and Output Filter Frequency Characteristics



Source Parameters

$f = 2.45 \times 10^9$ Hz (2.45 GHz)

$V_{am} = 25$V (1.04W input)

Input Filter Parameters

$C_{11} = 1.40$ pF, $C_{13} = 2.09$ pF

$L_{12} = 5.70$ nH, $L_{14} = 5.70$ nH

$R_{12} = 0.66$ ohms, $R_{14} = 0.66$ ohms

$C_{15} = 1.40$ pF

Output Filter Parameters

$L_{01} = 10.4$ nH

$R_{01} = 1.20$ ohms

$C_{02} = 10.75$ pF

Diode Parameters ($T = 300°$K)

$\phi = 0.8$ eV

$n = 1.0$

$C_j(0) = 0.7$ pF

$I_s = 10.0$ nA

$R_s = 0.50$ ohm

Antenna Parameters

$R_a = 75$ ohms

$L_a = 0$ nH

$C_a = 3$ pF

Input Transmission Line

$Z_{01} = 75$ ohms

$T_{01} = 51$ ps

Diode Package and Mount

$L_p = 0.3$ nH

$C_p = 0.2$ pF

$L_m = 0.5$ nH

$R_m = 0.25$ ohm

Output Transmission Line

$Z_{00} = 75$ ohms

$T_{00} = 0$ ps

Load

$R_L = 75$ ohms

Fig. 5 Computer Simulation Model for Rectenna RF to DC Conversion Circuitry

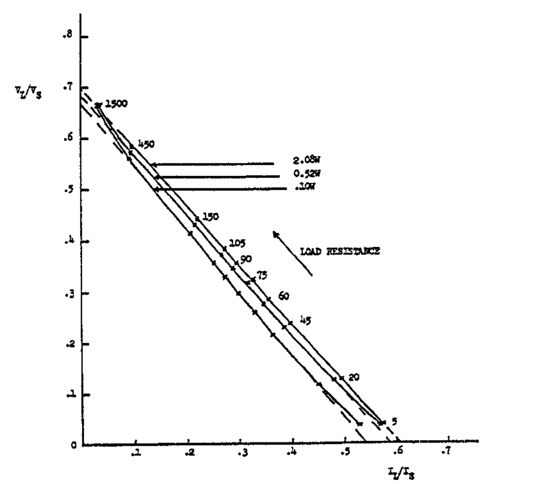


Fig. 6 Normalized Load Line from Computer Simulation Model

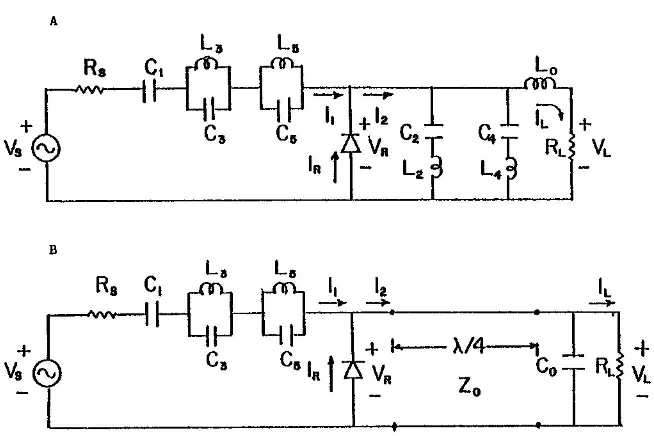


Fig. 3 Realizations of High Efficiency Rectifier Circuit

Power Combining Inefficiency (percent)

	Computer Simulation Model: Series Combining	Computer Simulation Model: Parallel Combining	Closed Form Model
10% at .5W, 90% at 2.0W	2.61	2.52	2.43
50% at .5W, 50% at 2.0W	10.83	10.51	10.00
90% at .5W, 10% at 2.0W	7.68	7.51	6.92
Uniform distribution .5W to 2.0W	3.98	3.87	3.67
Uniform distribution .5W to 1.4W	2.62	2.55	2.40

Table 1 Power Combining Inefficiency using Computer Simulation Model and Closed Form Model.